A rapid timing fixing methodology including impact of voltage drop to identify real timing violations.

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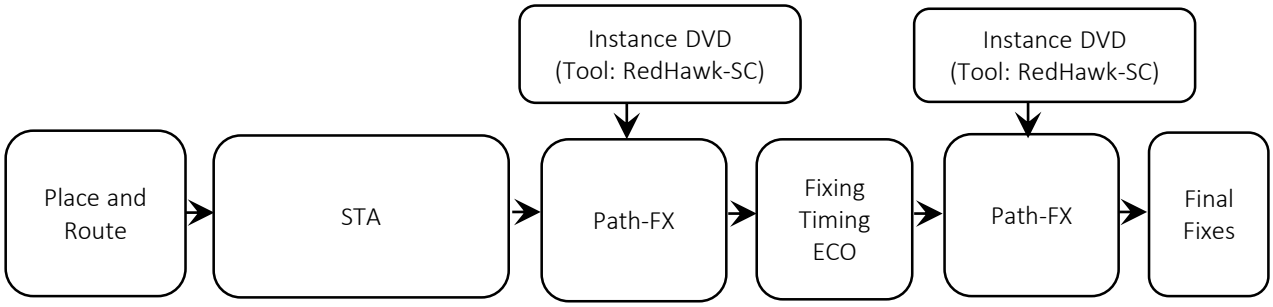
Motivation

- Existing timing closure methodologies for advanced technology nodes have additional margins to account for the increasing complexity of electrical effects such as on-chip variation (OCV), statistical OCV, signal integrity etc. as well as to include the effect of dynamic voltage drops on timing which is significant at these advanced nodes.

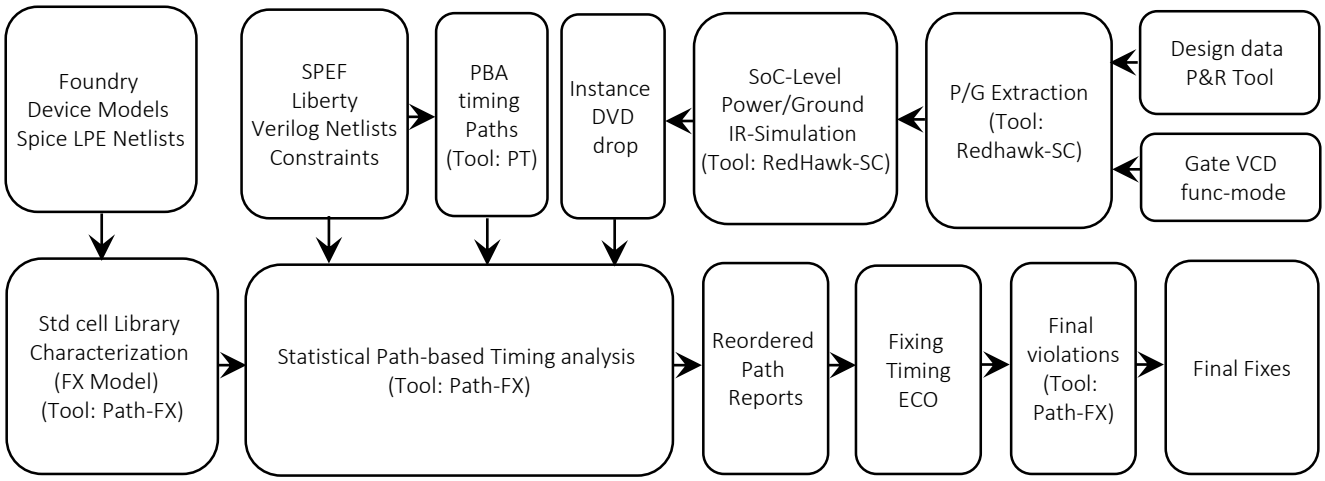
- Not only does the addition of above margins add pessimism and overdesign, it also increases turn around time to identify real violations. The current methodologies starting from course graph-based analysis (GBA) in initial stages, to accurate path-based analysis (PBA) with static timing analysis (SSTA) in final sign-off stages followed by Monte-Carlo SPICE to identify real violations, easily takes several days of ECO for timing-fixing.

- We present a timing fixing methodology and results on an SoC that improves existing margin-based approach to minimize overdesign through fast and high capacity transistor-accurate path based analysis to rapidly identify the real violations, reducing days of ECO down to hours.

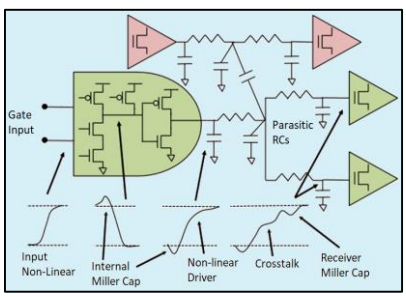
Methodology

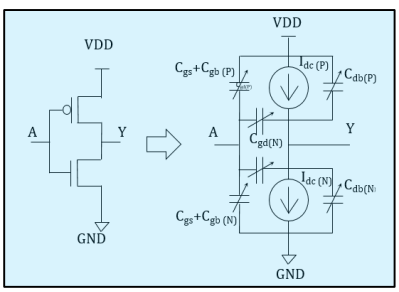


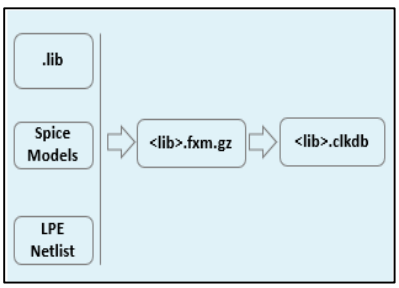
(a) Methodology : flow



(b) Flow steps







- The std cell libraries are characterized using FX Model generation which is a fast process that incorporates foundry process models and transistor layout to get a detailed model of cell behavior. The model captures high-risk timing behaviors like multiple input switching, non-linear input slews, voltage drop, functional noise, and Miller capacitance
- The power ground dynamic IR drop on instances is simulated using functional VCDs and fed to statistical timing analysis simulator
- The path based statistical timing analysis is threaded and distributed to reduce turn around time compared to MC-Spice

Results

- The accuracy and runtimes were compared on worst 10 timing paths between Hspice Monte Carlo SPICE vs Path FX tool

Path-FX Statistical Path Delay Accuracy versus Hspice Monte Carlo (1000 Samples)								
Path Number	Path Type	Hspice mean (ps)	Hspice 3-sigma (ps)	Hspice combined (ps)	Path FX mean (ps)	Path FX variation (ps)	Path FX combined (ps)	Statistical % Error
path1	launch	897.6796	9.984	887.6956	903.12203	-10.9	892.22203	0.510%
path2	launch	927.3364	9.8979	917.4385	937.91167	-10.7	927.21167	1.065%
path3	launch	905.1717	9.9408	895.2309	905.97627	-10.6	895.37627	0.016%
path4	launch	927.3434	9.9654	917.378	932.15219	-10.9	921.25219	0.422%
path5	launch	923.4586	9.3285	914.1301	928.2006	-10.4	917.8006	0.402%
path6	launch	908.6914	10.029	898.6624	915.48112	-10.7	904.78112	0.681%
path7	launch	978.5914	9.885	968.7064	980.1649	-11.1	969.0649	0.037%
path8	launch	918.7042	10.0848	908.6194	919.70648	-11	908.70648	0.010%
path9	launch	906.2029	10.0869	896.116	911.7816	-10.7	901.0816	0.554%
path10	launch	924.789	12.408	912.381	927.4373	-12.6	914.8373	0.269%

Path-FX Statistical Path Delay Accuracy versus Hspice Monte Carlo (1000 Samples)								
Path Number	Path Type	Hspice mean (ps)	Hspice 3-sigma (ps)	Hspice combined (ps)	Path FX mean (ps)	Path FX variation (ps)	Path FX combined (ps)	Statistical % Error
path1	capture	770.3121	6.4332	776.7453	778.22946	7.500	785.72946	1.157%
path2	capture	818.1088	8.9472	827.056	824.37363	9.700	834.07363	0.849%
path3	capture	811.2669	6.4185	817.6854	819.97417	7.600	827.57417	1.209%
path4	capture	819.028	6.7548	825.7828	823.20809	7.800	831.00809	0.633%
path5	capture	814.2607	8.1867	822.4474	818.79665	9.400	828.19665	0.699%
path6	capture	794.4538	8.2584	802.7122	798.97389	9.100	808.07389	0.668%
path7	capture	862.247	8.1957	870.4427	874.01178	9.800	883.81178	1.536%
path8	capture	807.3791	6.8652	814.2443	809.67933	8.000	817.67933	0.422%
path9	capture	807.3266	6.9294	814.256	812.16107	8.100	820.26107	0.737%
path10	capture	795.7908	7.9647	803.7555	802.31483	9.600	811.91483	1.015%

- The accuracy was found within 2% of MC Spice with orders of magnitude improvements in runtimes.

RunTimes for above paths	Hspice Monte Carlo	Path FX Statistical
Launch Paths	59 Hr 48 Min	0 Hr 7 Min
Capture Paths	53 Hr 38 Min	0 Hr 6 Min

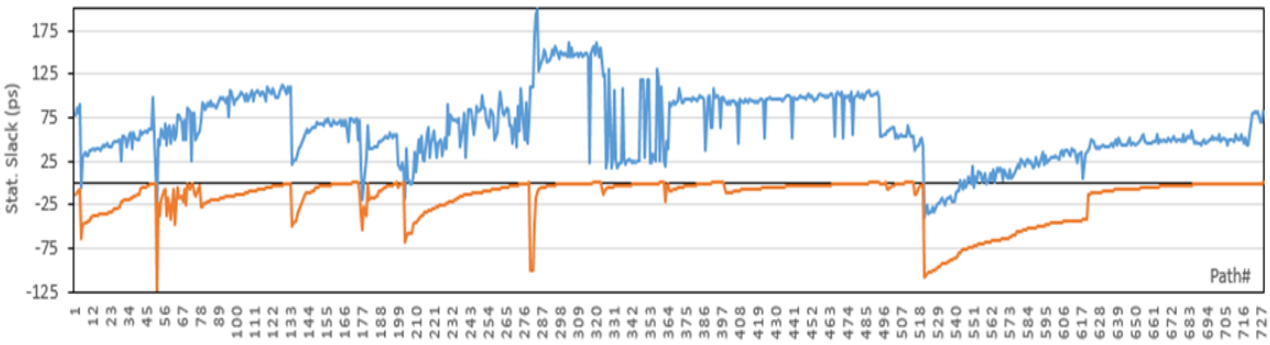
- The total number of negative statistical slack violations reduced drastically from 780 to 55

Number of statistical slack violations	
Existing methodology	780
New methodology	55

- This can save days of total turn around time (TAT) for timing fixing.

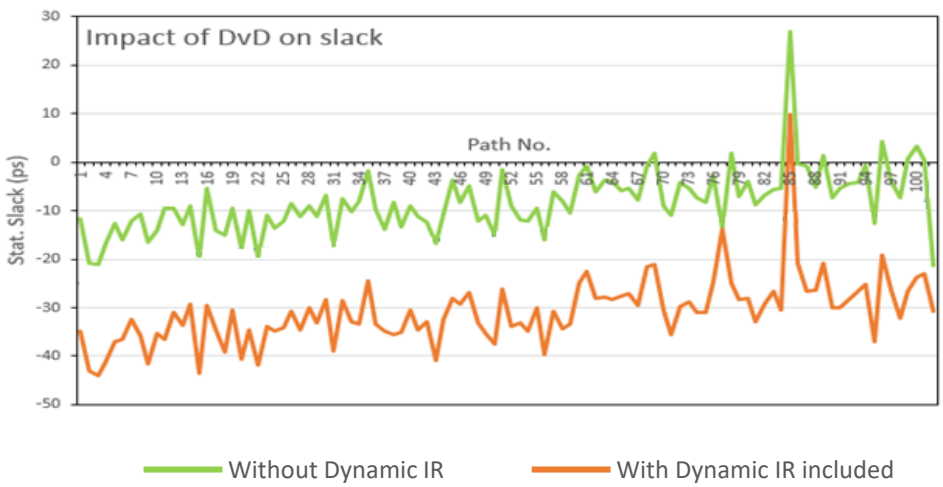
Results

- A comparison of statistical slack difference for identical negative slack violation paths shows increased pessimism due to margin based approach in the existing methodology.



Walltime	1 Hr 51 Min
Memory	185 GB

- The effect of dynamic voltage drop on cell delays and subsequently statistical slack is significant for this SoC on advanced technology node.



Summary

- We present a timing fixing methodology including impact of dynamic voltage drop that improves upon existing margin-based approach to minimize overdesign and pessimism in existing timing closure flow.

- The methodology leverages transistor SPICE models to create new (FX) models of the std cell libraries that work with a fully statistical simulator to accurately model delays, slews, constraints and the non-gaussian behavior. The simulator is threaded and distributed to reduce turn around time compared to MC-Spice

- Our results for an SoC on advanced technology node, when compared with existing margin-based flow clearly reveal the pessimism in the number of violations identified. The accuracy of the results was found within 2% of MC-Spice with orders of magnitude reduction in runtimes, resulting is rapid identification of real violations.